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Claim 1 (currently amended): A method of forming a damascene interconnect structure in a semiconductor integrated circuit, the method comprising:

forming a trench in a first dielectric layer on a substrate;

forming a dielectric diffusion barrier film in the trench for preventing the diffusion of a copper interconnect metal layer into the first dielectric layer;

etching the dielectric diffusion barrier film anisotropically to remove the dielectric barrier film from the bottom surface of the trench to expose patterned metal;

depositing a barrier metal film in the trench to cover at least a portion of the bottom surface exposed by etching, wherein the thickness of the barrier metal film formed on the sides of the trench is approximately 20 per cent or less of the thickness of the barrier metal film formed at the bottom of the trench; and

filling the trench with a copper interconnect metal layer.

Claim 2 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, further comprising forming a via aligned with the trench before forming a dielectric diffusion barrier film in the trench and wherein forming the dielectric diffusion barrier film in the trench is formed substantially simultaneously with the formation of the dielectric diffusion barrier film in the via.

Claim 3 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the dielectric copper diffusion barrier layer is formed by one of CVD, PECVD, MOCVD, and ALD methods.

Claim 4 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the barrier metal film further covers the sides of the trench.

Claim 5 (cancelled).

Claim 6 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the wherein the thickness of the barrier metal film formed on the sides of the trench is approximately 10 per cent or less of the thickness of the barrier metal film formed at the bottom of the trench.

Claim 7 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the thickness of the barrier metal film formed on the bottom of the trench lies in the range of 10 to 100 Angstroms.

Claim 8 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the thickness of the dielectric diffusion barrier film deposited lies in the range of 15 to 500 Angstroms.

Claim 9 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the thickness of the dielectric diffusion barrier film lies in the range of 50 to 100 Angstroms.

Claim 10 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, further comprising depositing a copper seed layer on the barrier metal layer prior to filling the trench with copper.

Claim 11 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 10, wherein depositing a copper adhesion promoter occurs before depositing the copper seed layer.

Claim 12 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the trench is continuously lined with at least one of the dielectric diffusion barrier film or metallic diffusion barrier layer.

Claim 13 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the dielectric diffusion barrier film includes at least one of SiC, SiN, Boron Nitride, amorphous carbon, AlN and SiOC.

Claim 14 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the dielectric diffusion barrier film is formed by surface treating the dielectric layer using high density plasma bombardment to direct Ar or H_2 particles to the dielectric layer.

Claim 15 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the anisotropic etching of the diffusion barrier film is performed by a plasma etch.

Claim 16 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 1, wherein the barrier metal deposition is controlled by a directional deposition of the barrier metal.

Claim 17 (original): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 16, wherein the directional deposition is performed using one of ionized metal plasma (IMP), high power self-ionized plasma (SIP), physical vapor deposition (PVD), and ionized physical vapor deposition (IPVD) methods.

Claim 22 (new): The method of forming a damascene interconnect structure in a semiconductor integrated circuit as recited in claim 16, wherein the directional deposition is performed using one of ionized metal plasma (IMP), high power self-ionized plasma (SIP), and ionized physical vapor deposition (IPVD) methods.